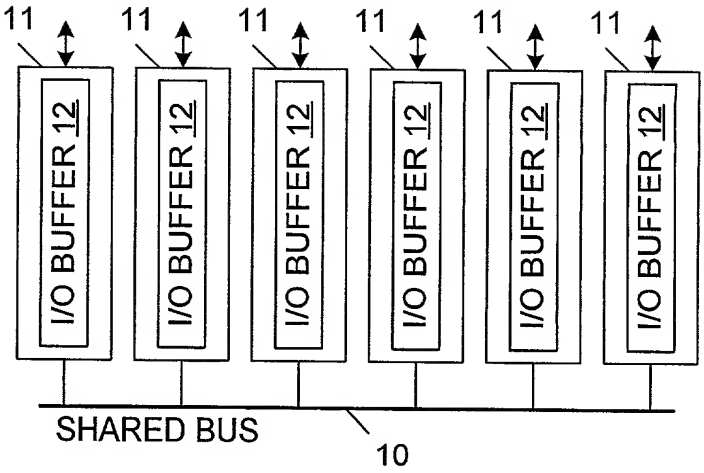

FIG. 1A
(PRIOR ART)

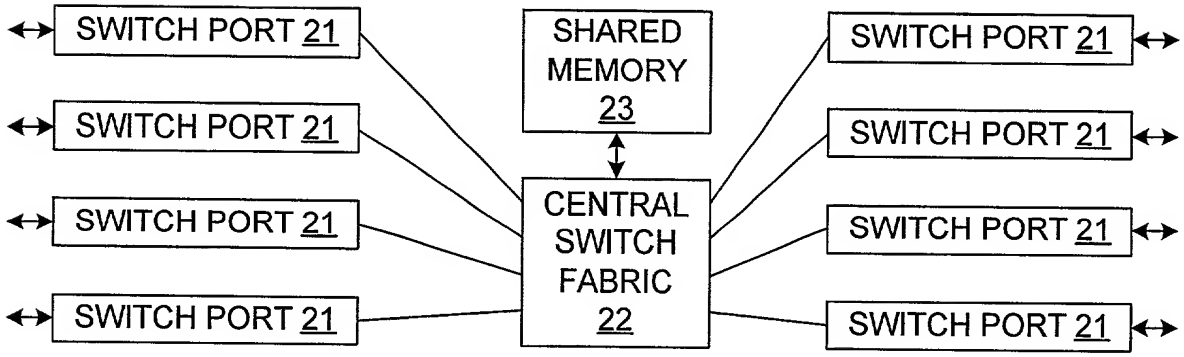

FIG. 1B
(PRIOR ART)

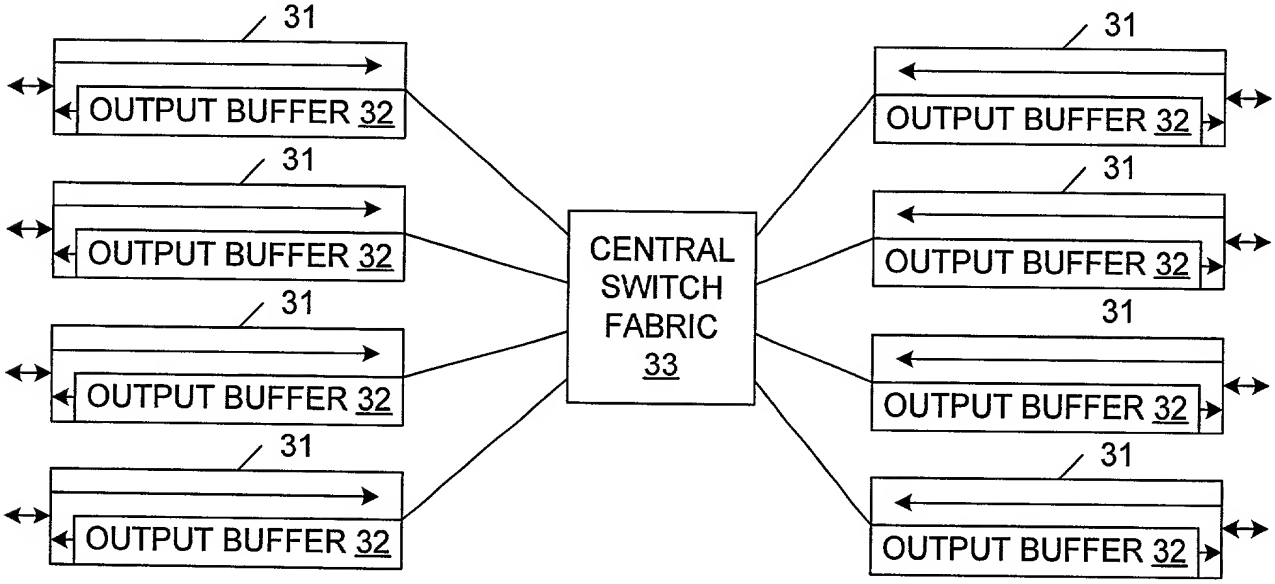

FIG. 1C
(PRIOR ART)

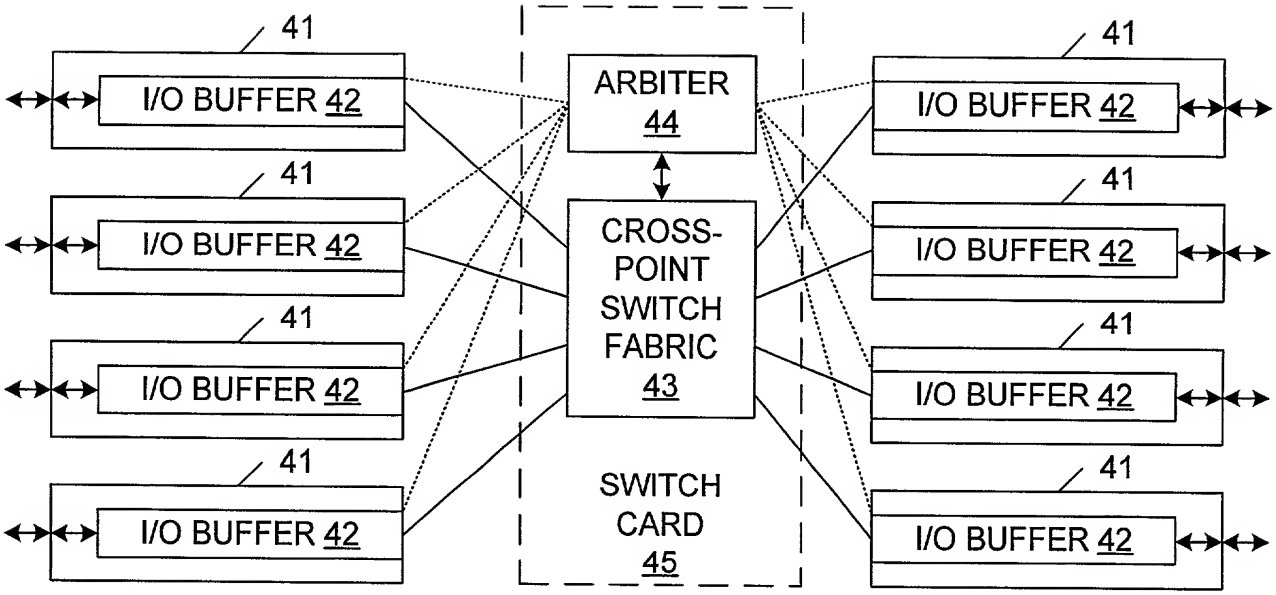

FIG. 1D
(PRIOR ART)

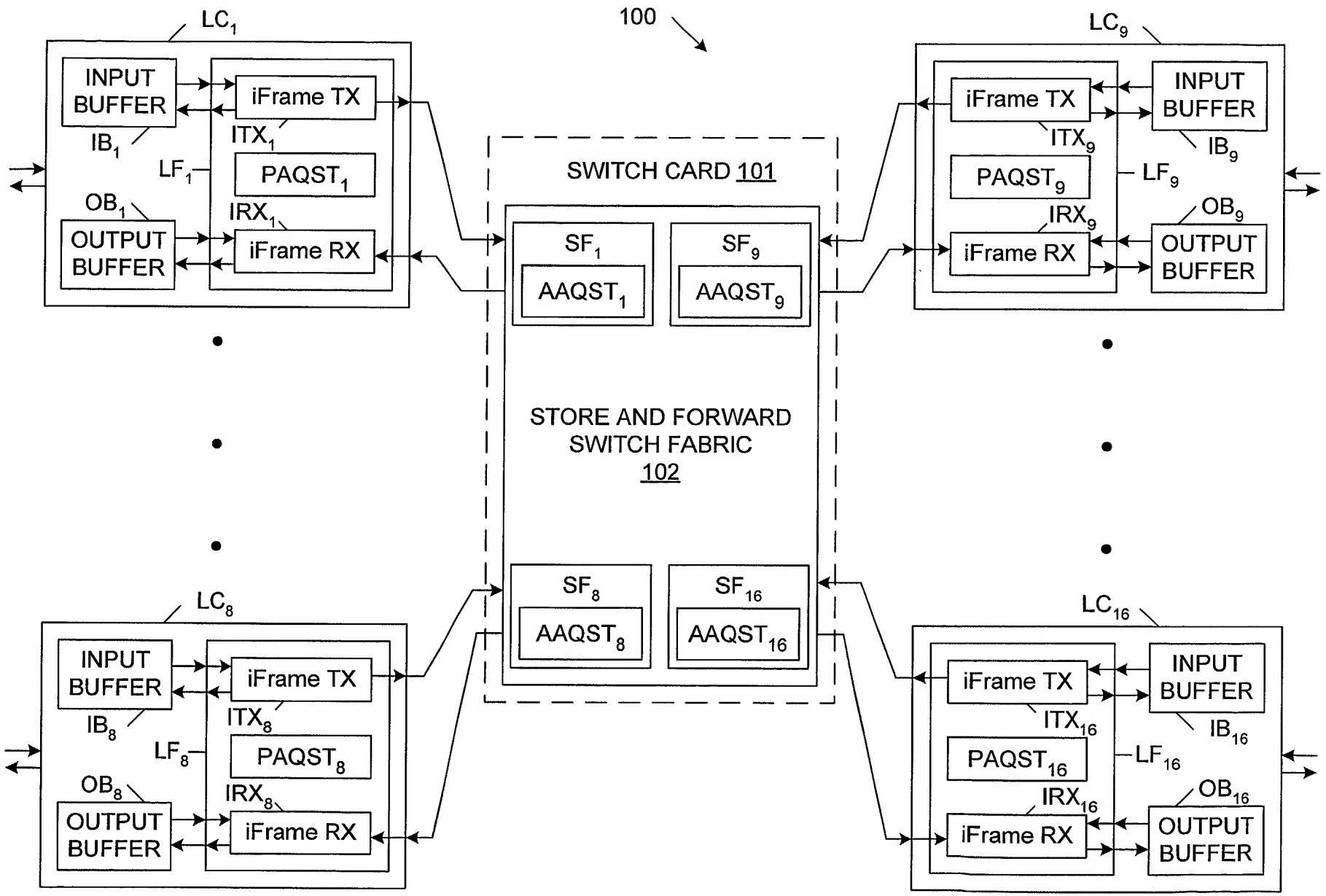
100
LC1
INPUT BUFFER
IB1
iFrame TX
ITX1
PAQST1
LF1
OB1
OUTPUT BUFFER
IRX1
iFrame RX
SWITCH CARD 101
SF1
AAQST1
SF9
AAQST9
STORE AND FORWARD SWITCH FABRIC 102
SF8
AAQST8
SF16
AAQST16
LC9
iFrame TX
ITX9
INPUT BUFFER
IB9
PAQST9
LF9
IRX9
iFrame RX
OB9
OUTPUT BUFFER
LC8
INPUT BUFFER
IB8
iFrame TX
ITX8
PAQST8
LF8
OB8
OUTPUT BUFFER
IRX8
iFrame RX
LC16
iFrame TX
ITX16
INPUT BUFFER
IB16
PAQST16
LF16
IRX16
iFrame RX
OB16
OUTPUT BUFFER

FIG. 2

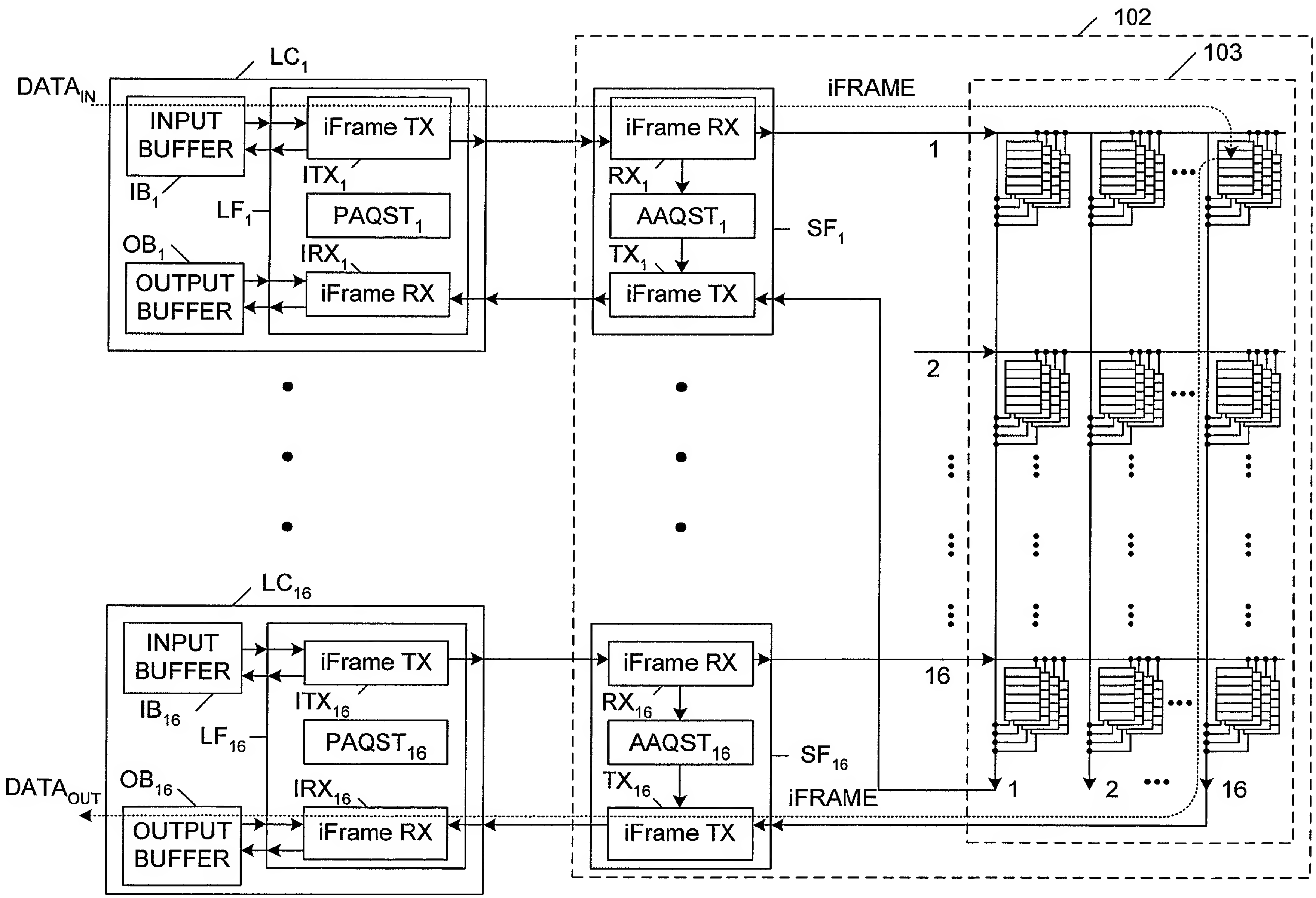
102
103
DATA$_{IN}$
LC$_1$
INPUT BUFFER
IB$_1$
iFrame TX
ITX$_1$
LF$_1$
PAQST$_1$
OB$_1$
OUTPUT BUFFER
IRX$_1$
iFrame RX
iFrame RX
RX$_1$
AAQST$_1$
TX$_1$
iFrame TX
SF$_1$
iFRAME
1
2
16
LC$_{16}$
INPUT BUFFER
IB$_{16}$
iFrame TX
ITX$_{16}$
LF$_{16}$
PAQST$_{16}$
DATA$_{OUT}$
OB$_{16}$
OUTPUT BUFFER
IRX$_{16}$
iFrame RX
iFrame RX
RX$_{16}$
AAQST$_{16}$
TX$_{16}$
iFrame TX
SF$_{16}$
iFRAME
1
2
16

FIG. 3

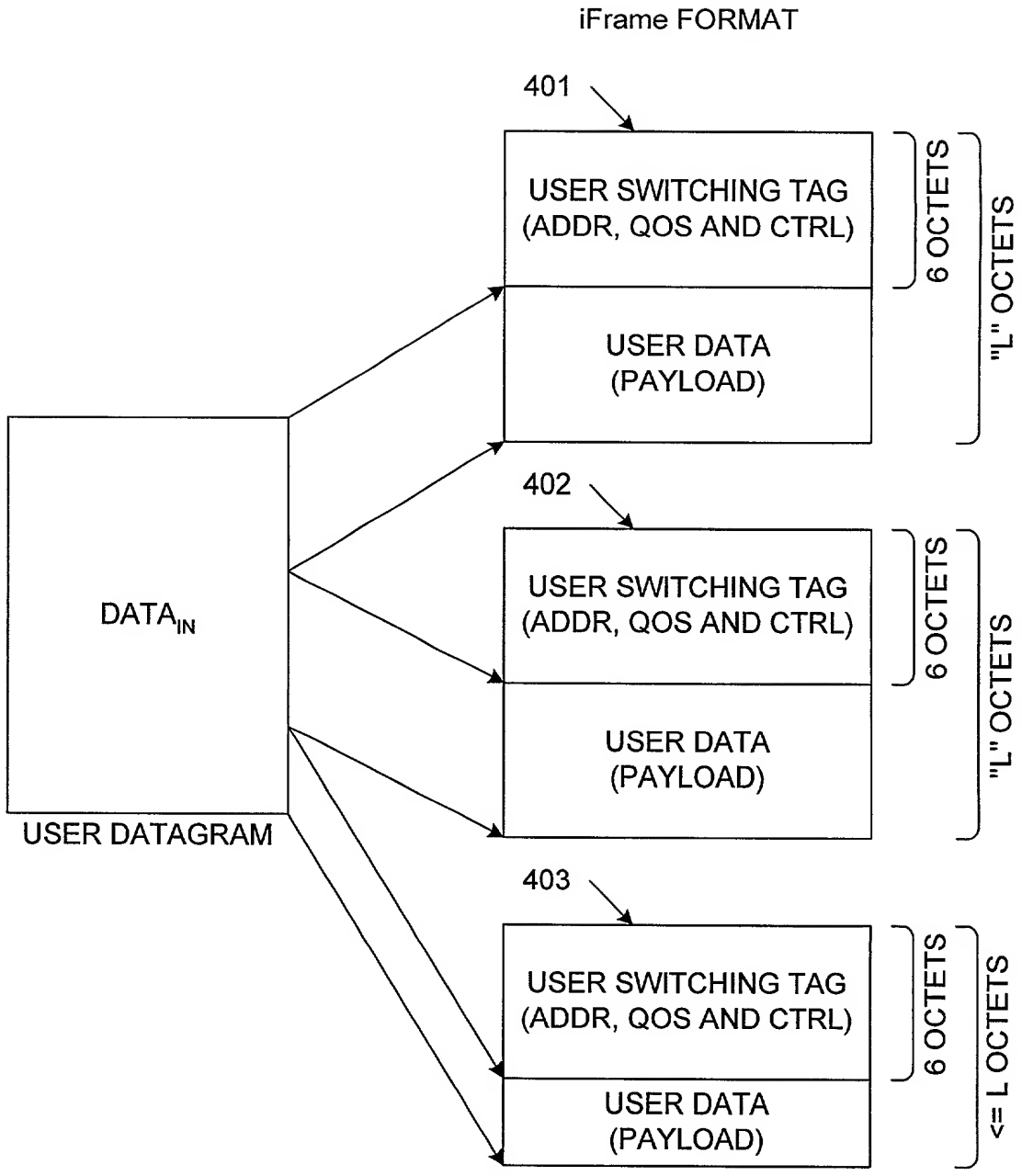
iFrame FORMAT
401
USER SWITCHING TAG
(ADDR, QOS AND CTRL)
6 OCTETS
USER DATA
(PAYLOAD)
"L" OCTETS
402
USER SWITCHING TAG
(ADDR, QOS AND CTRL)
6 OCTETS
USER DATA
(PAYLOAD)
"L" OCTETS
403
USER SWITCHING TAG
(ADDR, QOS AND CTRL)
6 OCTETS
USER DATA
(PAYLOAD)
<= L OCTETS
DATA_IN
USER DATAGRAM

FIG. 4

501A

INGRESS USER SWITCHING TAG FOR UNICAST IFRAMES

C1 (1-bit)	C2 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	F (1-bit)	L (1-bit)	EGRESS PORT QoS (2-bit)
EGRESS SWITCH PORT ID (8-bit)						
FLOW ID (8-bit)						
FLOW ID (8-bit)						
FLOW ID (6-bit)						RESERVED = 00 (2-bit)
TEC (CRC OR PARITY CHECK) (8-bit)						

FIG. 5A

501B

INGRESS USER SWITCHING TAG FOR MULTI-CAST IFRAMES

C1 (1-bit)	C2 (1-bit)	M=1 (1-bit)	E=0 (1-bit)	F (1-bit)	L (1-bit)	EGRESS PORT QOS (2-bit)
16-bit DIRECT MULTI-CAST EGRESS SWITCH PORT IDs (8-bit)						
16-bit DIRECT MULTI-CAST EGRESS SWITCH PORT IDs (8-bit)						
14-bit MCID CONTINUED (8-bit)						
14-bit MCID CONTINUED (6-bit)						RESERVED = 00 (2-bit)
TEC (CRC OR PARITY CHECK) (8-bit)						

FIG. 5B

EGRESS USER SWITCHING TAG FOR
UNICAST IFRAMES

601A

C1 (1-bit)	C2 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	F (1-bit)	L (1-bit)	PQS UPDATE QOS (2-bit)
PQS UPDATE ID (8-bit)						
22-bit FLOW ID (8-bit)						
22-bit FLOW ID (8-bit)						
22-bit FLOW ID (6-bit)						RESERVED = 00 (2-bit)
TEC (CRC OR PARITY CHECK) (8-bit)						

FIG. 6A

EGRESS USER SWITCHING TAG FOR
MULTI-CAST IFRAMES

601B

C1 (1-bit)	C2 (1-bit)	M=1 (1-bit)	E=0 (1-bit)	F (1-bit)	L (1-bit)	PQS UPDATE QOS (2-bit)
PQS UPDATE ID (8-bit)						
RESERVED = 0000 0000 (8-bits)						
14-bit MCID CONTINUED (8-bit)						
14-bit MCID CONTINUED (6-bit)						RESERVED = 00 (2-bit)
TEC (CRC OR PARITY CHECK) (8-bit)						

FIG. 6B

701A

INGRESS AAQSTj REQUEST CONTROL iFrame

C1=1 (1-bit)	C2=1 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	TYPE = 00 (2-bit)	RESERVED=00 (2-bit)
TEC (CRC OR PARITY CHECK) (8-bit)					

FIG. 7A

701B

INGRESS PURGE CONTROL iFrame

C1=1 (1-bit)	C2=1 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	TYPE = 01 (2-bit)	PQS QOS (2-bit)
PQSa ID (8-bits)					
• • •					
PQSn ID (8-bits)					
TEC (CRC OR PARITY CHECK) (8-bit)					

FIG. 7B

801A

$AAQST_J$ TABLE UPDATE

C1=1 (1-bit)	C2=1 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	F=0 (1-bit)	L=0 (1-bit)	TYPE=00 (2-bit)
4-bit $AQS_{J,1,1}$ UPDATE INCREMENT				4-bit $AQS_{J,1,2}$ UPDATE INCREMENT		
4-bit $AQS_{J,1,3}$ UPDATE INCREMENT				4-bit $AQS_{J,1,4}$ UPDATE INCREMENT		
4-bit $AQS_{J,2,1}$ UPDATE INCREMENT				4-bit $AQS_{J,2,2}$ UPDATE INCREMENT		
4-bit $AQS_{J,2,3}$ UPDATE INCREMENT				4-bit $AQS_{J,2,4}$ UPDATE INCREMENT		
•						
•						
•						
4-bit $AQS_{J,15,1}$ UPDATE INCREMENT				4-bit $AQS_{J,15,2}$ UPDATE INCREMENT		
4-bit $AQS_{J,15,3}$ UPDATE INCREMENT				4-bit $AQS_{J,15,4}$ UPDATE INCREMENT		
4-bit $AQS_{J,16,1}$ UPDATE INCREMENT				4-bit $AQS_{J,16,2}$ UPDATE INCREMENT		
4-bit $AQS_{J,16,3}$ UPDATE INCREMENT				4-bit $AQS_{J,16,4}$ UPDATE INCREMENT		
TEC (CRC OR PARITY CHECK) (8-bit)						

FIG. 8A

EGRESS PQS UPDATE CONTROL
iFrame

801B

C1=1 (1-bit)	C2=1 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	F=0 (1-bit)	L=0 (1-bit)	TYPE=01 (2-bit)
RESERVED = 00 (2-bits)		4-bit PQSa UPDATE INCREMENT				PQSa QOS (2-bit)
8-bit AQS/PQSa ID						

•
•
•

RESERVED = 00 (2-bits)	4-bit PQSn UPDATE INCREMENT	PQSn QOS (2-bit)
8-bit PQSn ID		
TEC (CRC OR PARITY CHECK) (8-bit)		

FIG. 8B

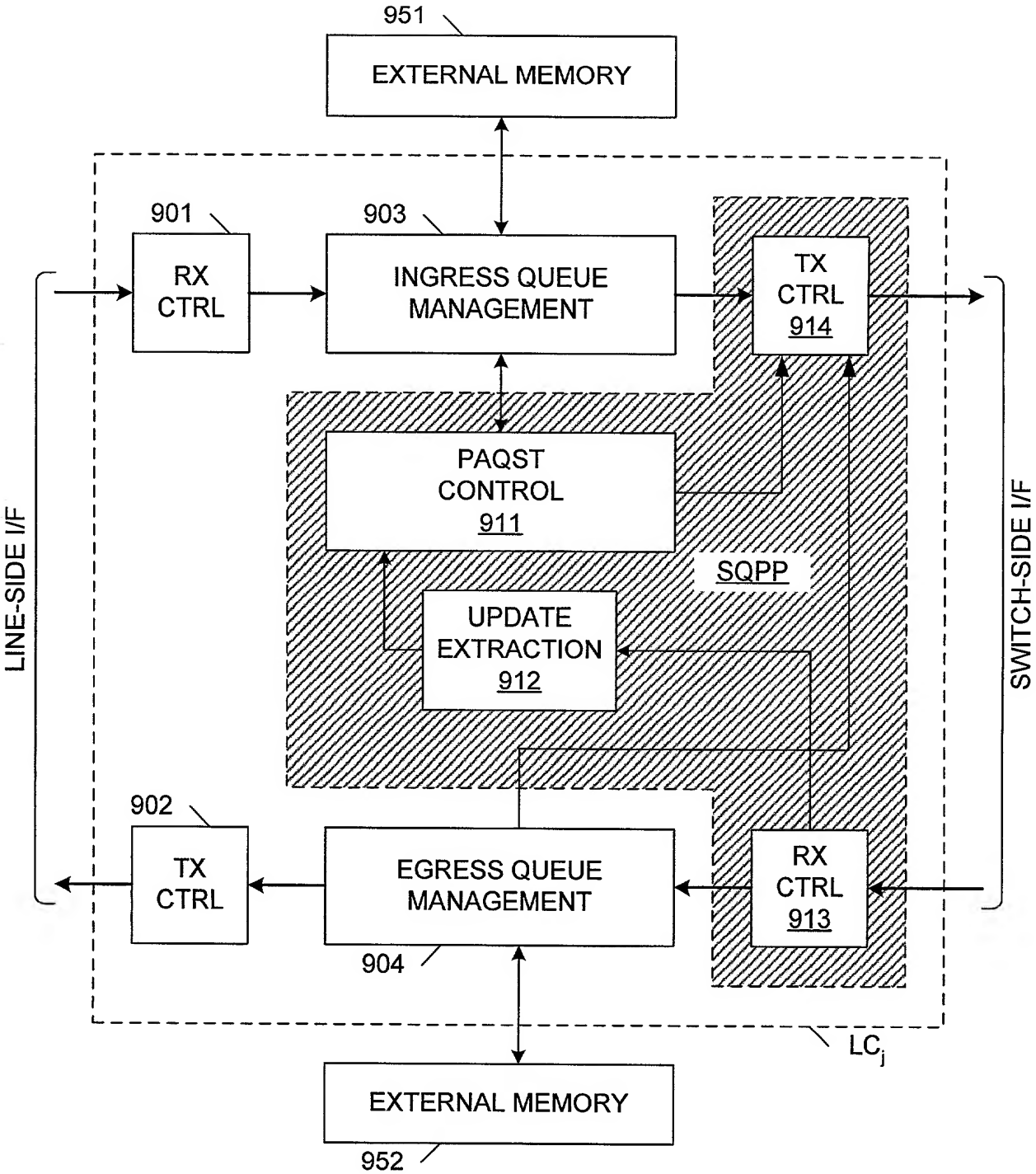
951
EXTERNAL MEMORY
901
RX CTRL
903
INGRESS QUEUE MANAGEMENT
TX CTRL 914
PAQST CONTROL 911
SQPP
UPDATE EXTRACTION 912
LINE-SIDE I/F
SWITCH-SIDE I/F
902
TX CTRL
EGRESS QUEUE MANAGEMENT
RX CTRL 913
904
LC$_j$
EXTERNAL MEMORY
952

FIG. 9

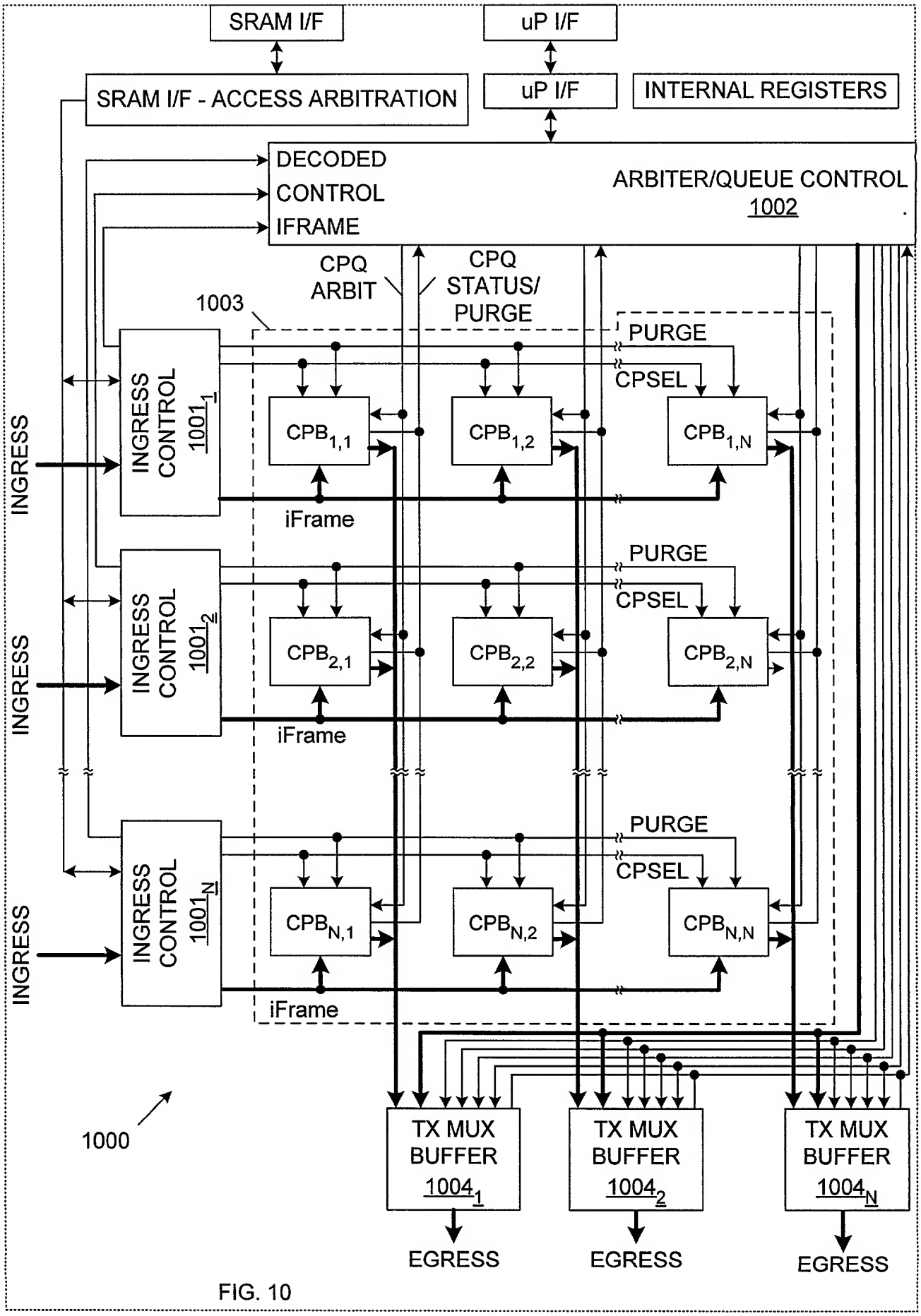
SRAM I/F
uP I/F
SRAM I/F - ACCESS ARBITRATION
uP I/F
INTERNAL REGISTERS
DECODED CONTROL IFRAME
ARBITER/QUEUE CONTROL 1002
CPQ ARBIT
CPQ STATUS/ PURGE
1003
PURGE
CPSEL
INGRESS
INGRESS CONTROL 1001_1
CPB1,1
CPB1,2
CPB1,N
iFrame
INGRESS CONTROL 1001_2
CPB2,1
CPB2,2
CPB2,N
INGRESS CONTROL 1001_N
CPBN,1
CPBN,2
CPBN,N
1000
TX MUX BUFFER 1004_1
TX MUX BUFFER 1004_2
TX MUX BUFFER 1004_N
EGRESS

FIG. 10